IES/GATE

Electrical Engineering

VOLUME-IX

Power Electronics

Contents

Power Electronics

1. Power Semiconductor Devices
2. Phase controlled rectifiers & applications (DC drives, charging battery, solar cells, HVDC :
3. SMPS DC → DC converters (Choppers).
4. SM DC → AC converters (Inverters)
5. Resonant converters; High frequency transformers & Inductors.

only for EES for PE., SMPS

AC Drives

Introduction → It deals with control and conversion of high power application with high efficiency.

* Power Semiconductor devices should be capable to handle very large magnitudes of power with high efficiency.

e.g; i) Power Diode
ii) SCR (Thyristor)
iii) LASCR (Light activated SCR)
iv) ASCR
v) RCT (Reverse conducting thyristor)
vi) GTO
vii) TRIAC
viii) DIAC
ix) Power transistors
- power BJT
- power MOSFET
- IGBT

* SCR & power diode handles highest power rating.
* MOSFET operates with highest switching frequency.

Signal Electronics →

* It deals with control of low power applications.
# Signal devices handles low power at very high switching frequency. e.g; Signal Diodes → LEDs, Zener diode, tunnel diode
Signal Transistors → BJT, UJT, MOSFET

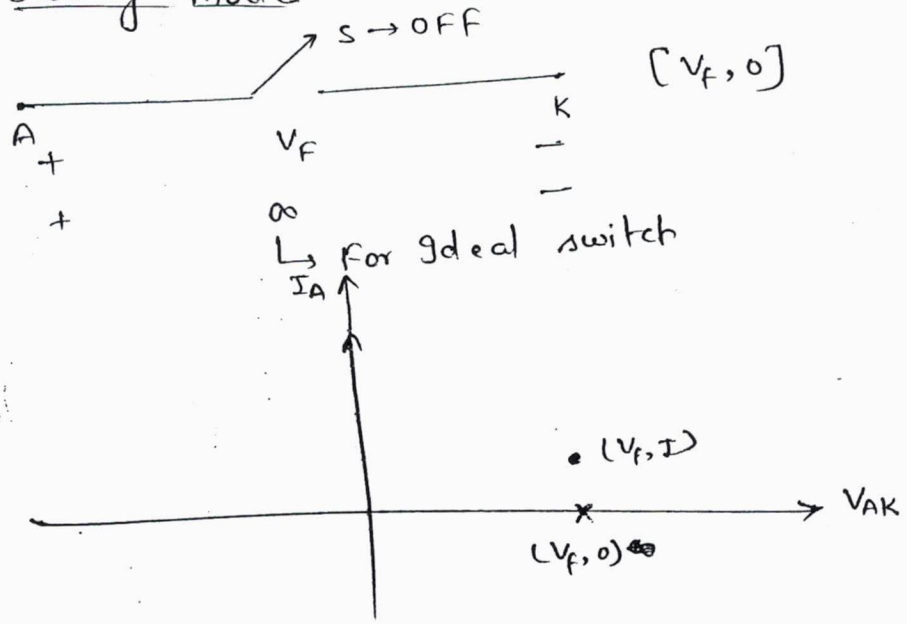
In PE the devices are mainly utilized at switches -
(i) Uncontrolled switch → e.g; Diode
(ii) Semicontrolled switch → eg; Anode, SCR
(iii) Fully controlled switch → e.g; GTO, MOSFET, IGBT

GTO

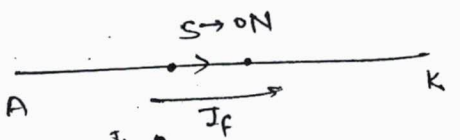
We can utilize a switch in 4 devices but all the devices need not to supports all the 4 for.

① Four modes of an ideal switch →

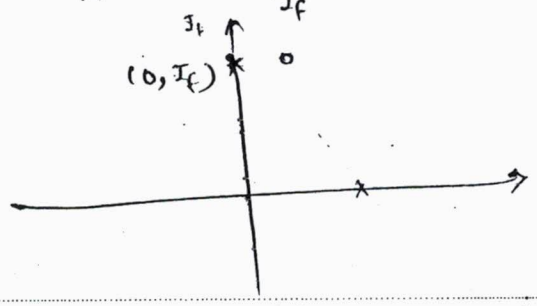
① Forward Blocking mode →



② Forward Conduction mode →

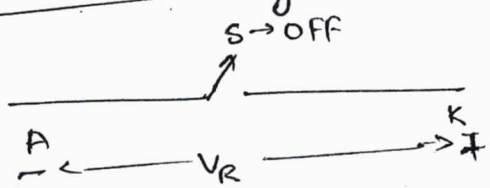


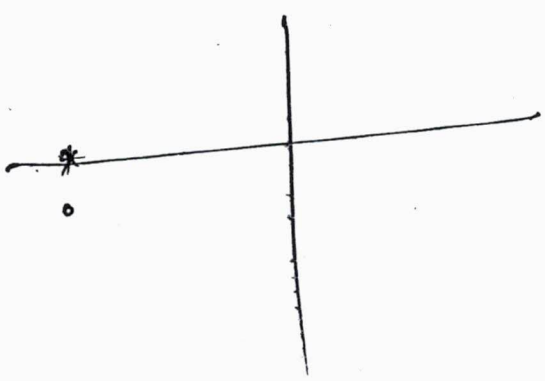
[0, If]



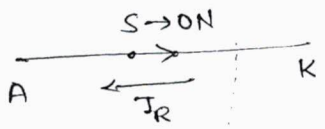
* Ideal
° Practical

③ Reverse Blocking case → [−VR, 0]

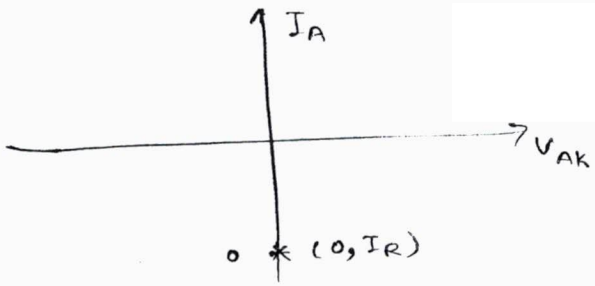


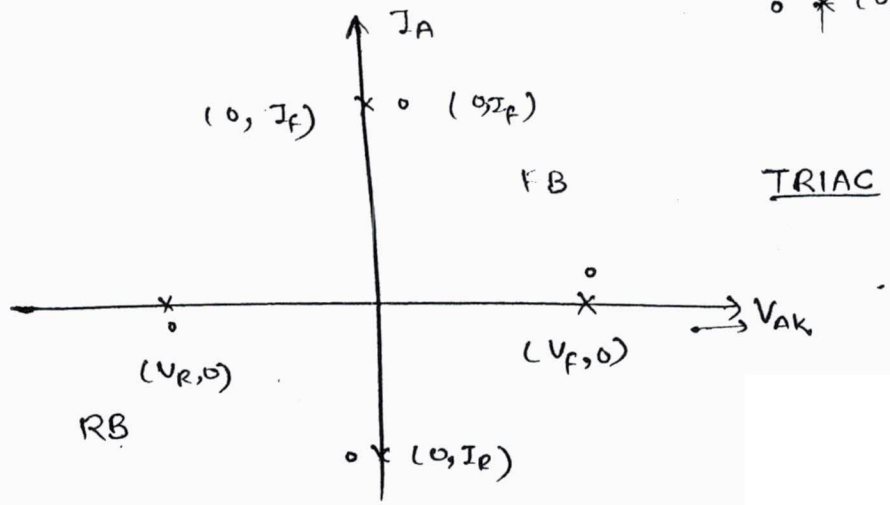


(iv) Reverse Conduction mode →



$[0, -I_R)$





Requirements of a Switch →

1) AC to AC conversion → The switch has to support all the four modes. TRIAC supports the 4 modes.

[FB, FC, RB, RC] ~~Vac~~ e.g; TRIAC

ii) AC to DC conversion →

The switch has to support the 3 parts.

~~No~~ SCR [FB, FC, RB]

Phase controlled rectifiers ~~X~~

AC ⟷ DC

Diode → fixed DC voltage.

iii) DC to DC conversion →

For DC → DC

[FB, FC) e.g; BJT, IGBT, SCR, GTO, TRIAC

iv) DC to AC conversion →

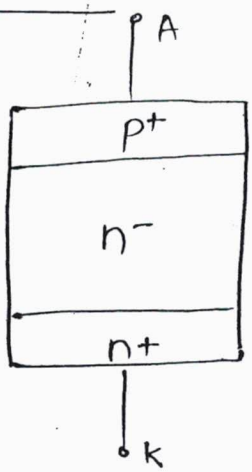
DC → AC

VSI
[FB, FC, RC]
(RCT)

CSI
[FB, FC, RB]
(SCR)

POWER SEMICONDUCTOR DEVICES

1. POWER DIODE →



Drift region

+ → Heavily dopped layer
− → lightly dopped layer

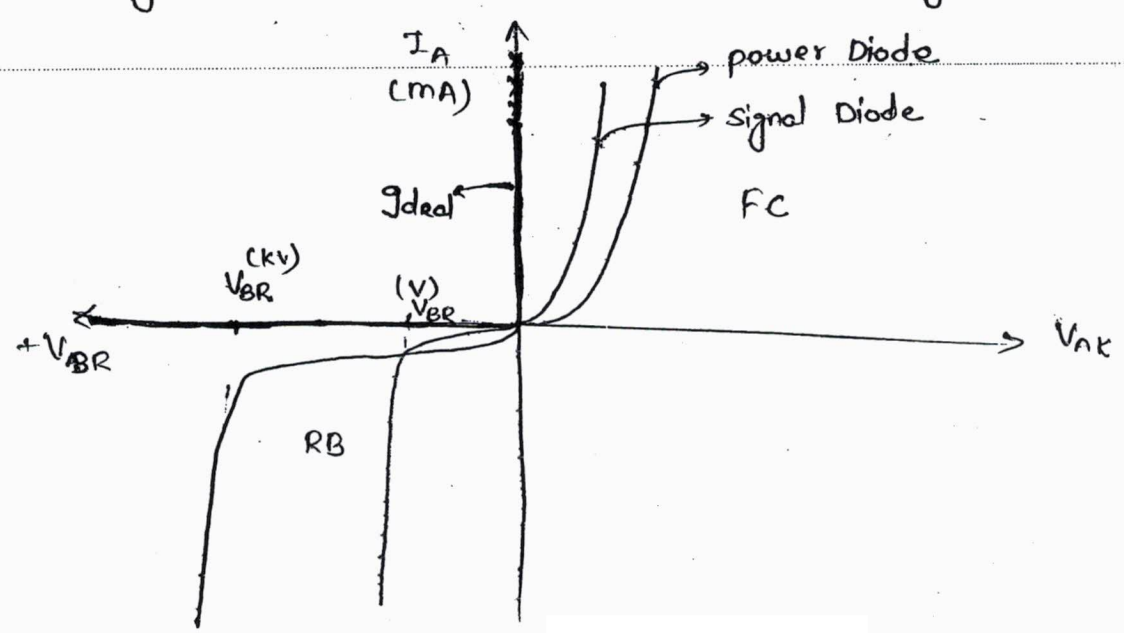
Reverse bias blocks the voltage
Forward bias supports the conduction.

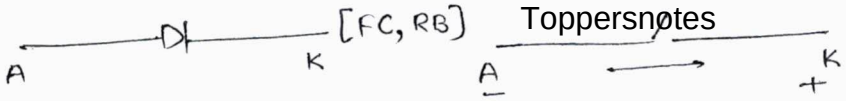
Significance of Drift Region →

† When anode is made −ve w.r. to cathode the depletion layer thickness increases very easily in the n^- layer. This increases the reverse blocking capability of a diode.

† The thickness of n^- layer decides the maximum thickness of depletion layer (higher the thickness of n^- layer, higher the reverse voltage it can block)

† The n-1 layer increases the ON state voltage drop of a diode.





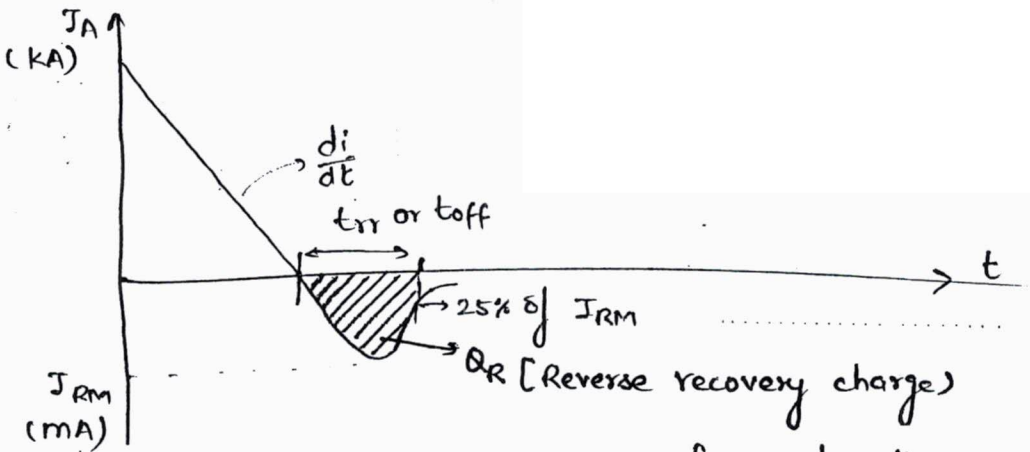
OFF ⟶ ON [t_{ON}]

ON ⟶ OFF [t_{off}]

$t_{off} >>> t_{ON}$

Reverse Recovery characteristics of Power Diode →

It explains the switching behaviour of a diode from ON state to OFF state.



When the diode is conducting in forward dir^n some excess charge carriers are stored in the device (these excess charge carriers are mainly due to minority carriers)

When the diode is switching from ON state to OFF state these excess charge carriers are still present in the diode even after the anode current becomes zero.

In order to remove these charge carriers and regain its normal state recombination process begins and hence reverse current flows in the diode untill all the charge carriers are completely removed.

This process is known as reverse recovery process and the transition time during this process is known as reverse recovery time (t_{rr})

$$Q_R = \frac{1}{2} t_{rr} \cdot I_{RM}$$

$$I_{RM} = \left[2 Q_R \frac{di}{dt}\right]^{1/2}$$

$$t_{rr} = \left[\frac{2Q_R}{di/dt}\right]^{1/2}$$

Q_R mainly depends on anode current magnitude when the diode is in ON state.

$$I_A \uparrow \Rightarrow Q_R \uparrow \Rightarrow I_{RM} \uparrow \Rightarrow t_{rr} \uparrow$$

t_{rr} decides the maximum switching frequency of a diode (for a diode if t_{rr} is high ⇒ switching frequency is less)

Classification of Power Diode based on t_{rr} →

① General Purpose Diode [Slow Diode]

② Fast Recovery Diode

③ Schottky Diode

General Purpose Diode	Fast Recovery Diode	Schottky Diode
1) t_{rr} = 25 μsec	t_{rr} → 5 μsec or less	t_{rr} → nano sec
2) Rating		
I_{rating} → 1A to several thousands of Amp.	$I_{ratings}$ → 1A to several hundreds of Amperes	$I_{ratings}$ → 300A
		$V_{ratings}$ → 100V
V_{rating} → 50V to 5KV (PIV)	V_{rating} → 50V to 3KV	

! In Fast recovery diodes the layers are dopped with gold or platinum.

Gold or Platinum dopping reduces the lifetime of charge carriers and increases its recombination speed this reduces the reverse recovery time and increases its switching frequency.

Schottky diode is a metal to semiconductor junction diode.

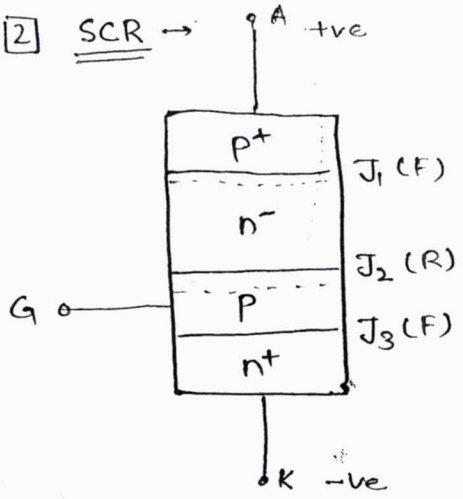
! In this diode conduction is only due to majority carriers (e^-)

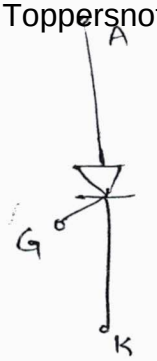
! Due to the absence of minority charge carriers the reverse recovery time is reduced very much and this diode operates with very very high switching frequency.

! Schottky diode is used in SMPS

! Fast recovery diodes generally used in inverters & choppers. General purpose diodes are generally used in line frequency rectifiers ∴ they are also known as rectifier diodes.

[2] SCR →





A, K → main terminals
G → Gate terminal (control terminal) (ON)

① Forward Blocking mode (FB)

Reverse biased junction blocks forward voltage

J_1, J_3 → Forward biased, J_2 → Reverse biased

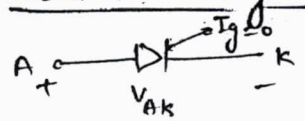
When Anode is +ve w.r.t to cathode J_1, J_3 → Forward B. & J_2 is reverse biased

∴ SCR remains in OFF state.

② Forward conduction mode (FC)

Triggering methods →

i) Forward voltage triggering method →



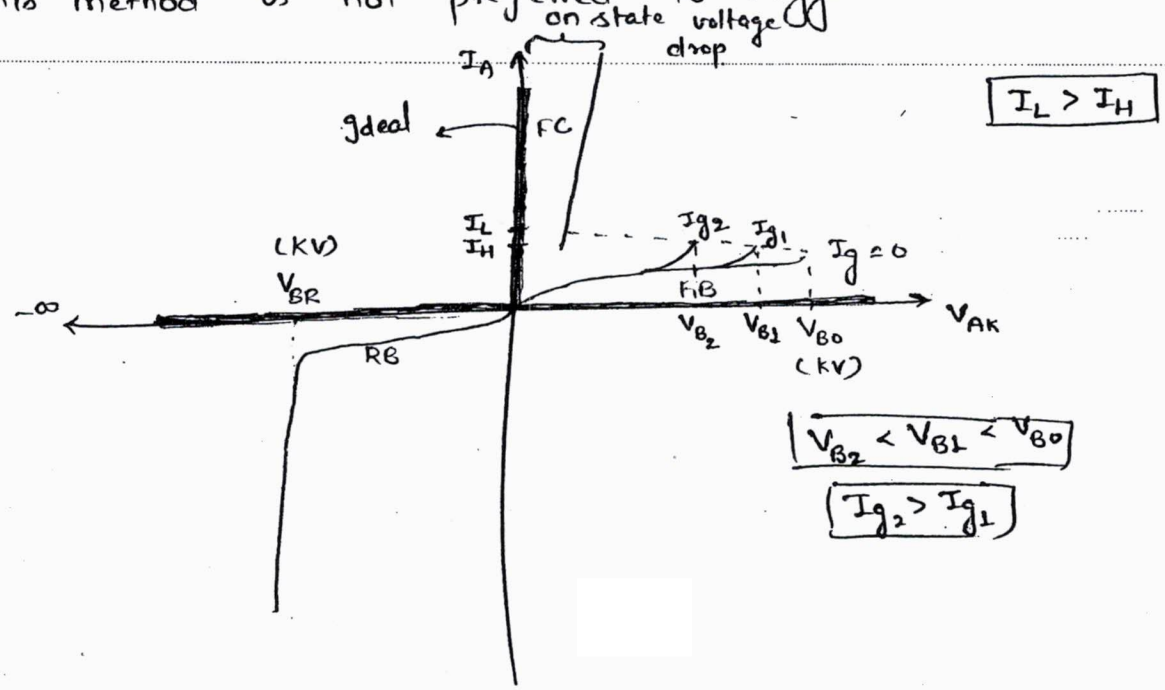
V_{AK} ↑ gradually upto V_{BO}

J_2 breaksdown for $V_{AK} > V_{BO}$

J_2 → FB

As the applied voltage (V_{AK}) increases and reaches V_{BO} breakdown occurs at J_2 ∴ SCR starts conducting

This method is not preferred to trigger the SCR.



$I_L > I_H$

$V_{B_2} < V_{B_1} < V_{BO}$

$I_{g_2} > I_{g_1}$

(ii) Gate triggering →

$I_{gmin} \leq I_g \leq I_{gmax}$

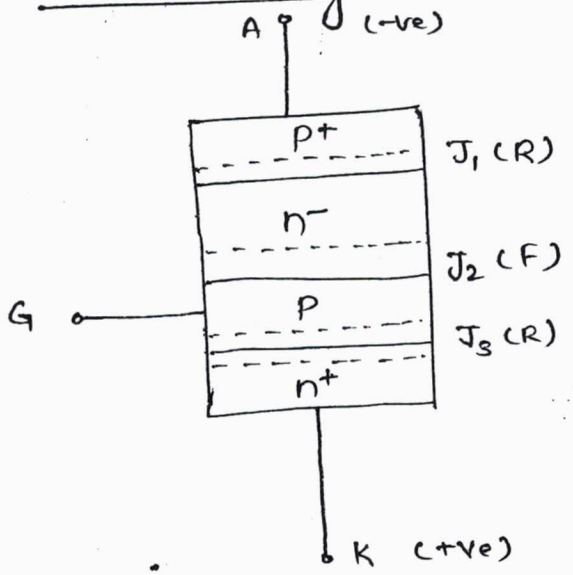
$V_{gmin} \leq V_g \leq V_{gmax}$

$I_g \uparrow$ or $\frac{dI_g \uparrow}{dt} \Rightarrow$ Initial conduction Area ↑

$\therefore \left(\frac{dI_a}{dt}\right) \uparrow$ Initial rate ↑

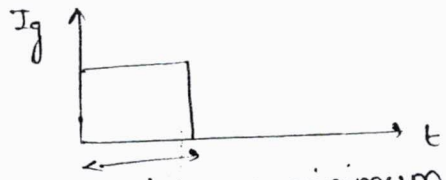
$\therefore t_{ON} \downarrow$ and $V_B \downarrow$ (Breakdown voltage V_B)

(B) Reverse Blocking Mode → (RB)



Significance of latching current →

- latching current is related to turn ON process.
- Gate signal initiates the turn ON process but once the device starts conducting, gate losses control on the device ∴ we can remove the gate pulse when SCR starts conducting to avoid the continous gate power loss.
- If we remove the gate pulse when anode current is less than latching current then SCR fails to turn ON. ∴ We must maintain the gate pulse width atleast for a period untill anode current reaches the latching current.



t_{min} → minimum gate pulse width required to turn ON the SCR.

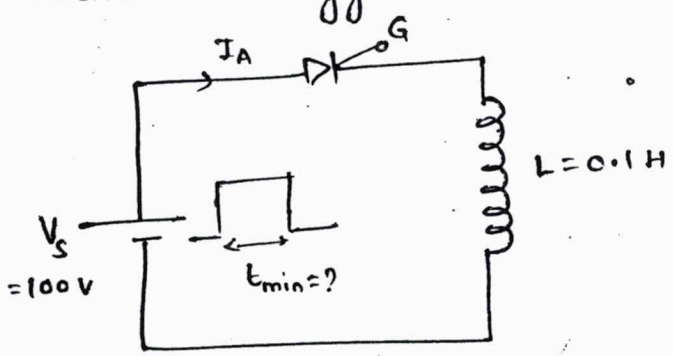
t_{min} : $\boxed{t_{gpw} > t_{min}}$, to turn ON SCR.

By using latching current we can find out the minimum gate pulse width required to turn ON the SCR.

Q. Calculate the minimum gate pulse width in the following circuits to trigger the SCR.

$V_S = 100V$

$I_L = 100mA$



Sol^n. KVL $\quad V_S = L\frac{dI_A}{dt}$

$$\int dI_A = \frac{V_S}{L}\int dt$$

$$i_A = \frac{V_S}{L}t$$

$$I_L = \frac{V_S}{L}t_{min}$$

$$t_{min} = \frac{I_L \cdot L}{V_S}$$

$$= \frac{100\times10^{-3}\times 0.1}{100}$$

$$= 10^{-4}\ sec$$

$$\Rightarrow \quad t_{min} = 100\ \mu sec$$

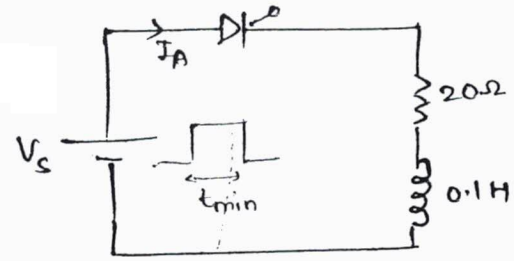
To turn ON the SCR $t_{gpw} \geq t_{min}$

$\therefore t_{gpw} \geq 100\ \mu sec$ Ans.

Note→ The minimum gate pulse width requirement depends on the load circuit parameters.

e.g.: If $L \uparrow\uparrow \Rightarrow t_{gpw} \uparrow\uparrow$ $\quad L = 0.2 \Rightarrow t_{min} = 200\ \mu sec$

Q.



$V_S = 100V$

$I_L = 100mA$

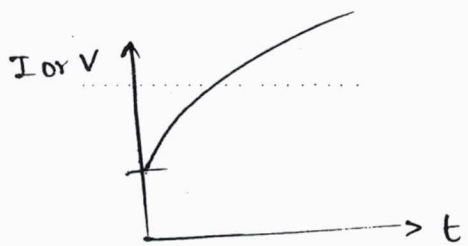
$t_{gpw} = ?$

Soln $\quad V_S = RI_A + L\frac{dI_A}{dt}$

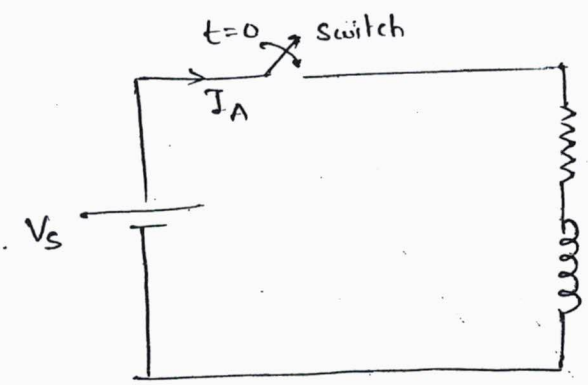
To find the natural response we replace the forcing function by its internal resistance.

$K_i \quad (t=0)$

$K_f \quad (t=\infty)$



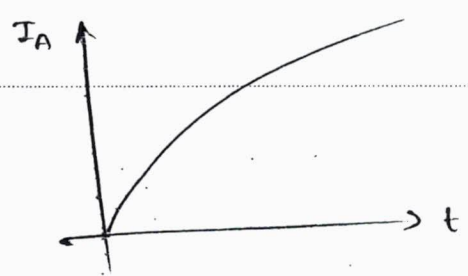
$$y = K_f(1-e^{-t/T}) + K_i e^{-t/T}$$



$i_A(t=0^-) = i_A(t=0^+) = 0$

$K_i = 0$

$K_f = \frac{V_S}{R}$ at $(t=\infty)$



$$i_A = \frac{V_S}{R}(1-e^{-t/T})$$

$$i_A = \frac{100}{20}(1-e^{-200t})$$

$$I_L = 5(1-e^{-200\,t_{min}})$$

$$t_{min} = 101\ \mu sec$$ Ans

latching current is related to turn ON process.

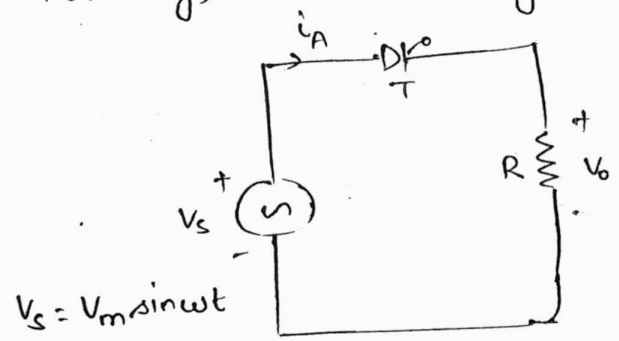
Significance of Holding current →

Holding current is related with turn OFF proces

Gate has no control to turn OFF the SCR.

SCR will turn OFF only when anode current ↓ below the holding current.

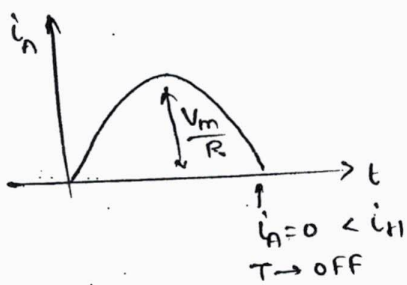
In some of the cases natural commutation is possible. For e.g; consider single phase half wave rectifier.



SCR → ON

$$i_A = \frac{V_s}{R}$$

$$i_A = \frac{V_m \sin\omega t}{R}$$



If supply is DC then natural commutation is not possible we must used forced commutation circuit to turn OFF the SCR if load commutation is not possible.

Commutation circuit reduce the anode current below the holding current and then apply a reverse voltage across the SCR atleast for a period untill all the charge carriers are completelly removed in the circuit. device completely.

Q. What is meant by circuit turn OFF time (t_c)?

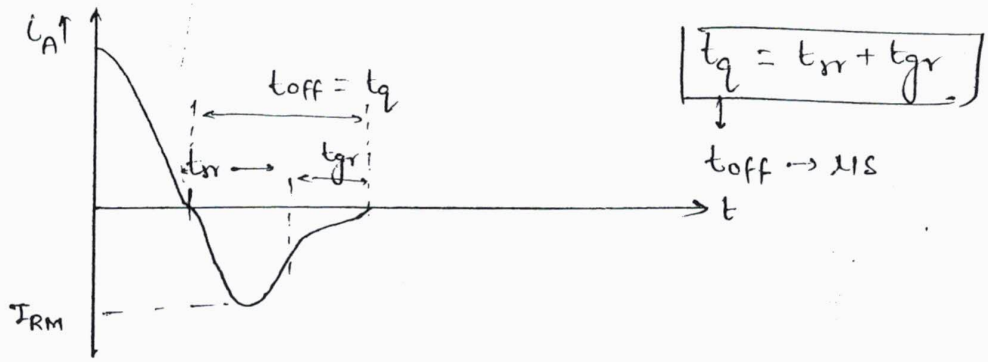
Soln It is the time for which commutation circuit supplies the reverse voltage across the SCR after anode current becomes zero.

t_q → turn off time for SCR

$t_c > t_q$ → for successfull commutation.

Reverse Recovery characterstics of SCR → [Turn OFF characterstics]

- It explains the switching behaviour of SCR from ON state to OFF state.



t_{rr} → Reverse recovery time → During this period the excess charge caniers present in the outer layer is removed.

t_{gr} → Gate recovery time → During this period the excess charge carriers present near the gate junction is removed.

t_q → Device turn off time → The turn OFF time of the SCR (t_q) decides the maximum switching speed of a thyristor.

- Thyristor

Converter Grade thyristor	Inverter grade thyristor
	Fast thyristors
• Slow thyristors	• t_q → 3 μs to 50 μs.
• t_q → 50 μs to 100 μs	• It is used in inverters and choppers
• Slow thyristors are used in line frequency rectifier and ACVC.	

If $t_c \geq t_q$ * → commutation is successfull.

↳ circuit turn OFF time

t_c = safety factor × t_q *

Safety factor > 1 *

- If $t_c < t_q$ commutation fails

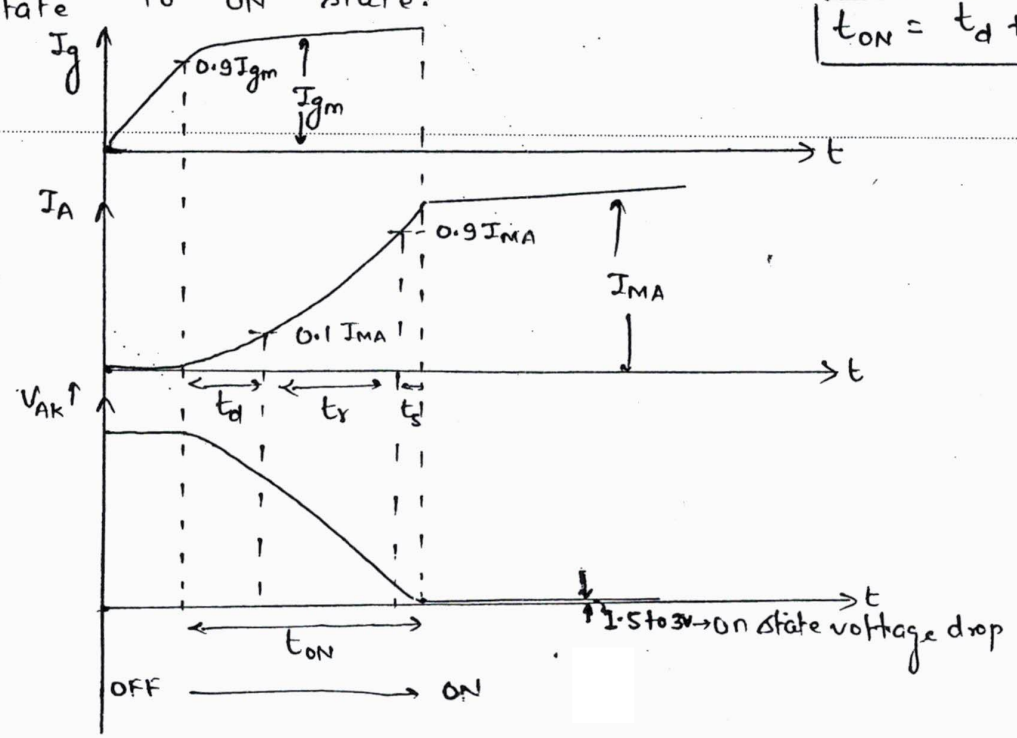
Q. What do you mean by commutation failure?

Sol" If $t_c < t_q$, some excess charges still present near the gate junction i.e; SCR did not regain its normal state. For the next operation if anode is made +ve w.r.t to cathode then SCR will turn ON immediately before the gate pulse is given. Here SCR behaves just like a diode losing its forward blocking capability. This is known as commutation failure. ∴ We must apply reverse voltage across the SCR atleast for a period untill all the charge carriers are completely removed.

Turn ON process →

- It explains the switching behaviour of SCR from OFF state to ON state.

$t_{ON} = t_d + t_r + t_s$



- Delay time (t_d) → t_d depends on gate signal magnitude I_g & $\frac{d}{dt} I_g$.

  $I_g \uparrow$ or $\frac{d}{dt} I_g \uparrow \Rightarrow$ initial conduction area $\uparrow \Rightarrow \left(\frac{d}{dt} I_A\right) \uparrow$ initial rate

  $\therefore t_d \downarrow \therefore t_{ON} \downarrow$

- Rise time (t_r) → t_r depends on load parameters.

  $L \uparrow \Rightarrow \frac{di}{dt} \downarrow$

  $\therefore t_r \uparrow \Rightarrow t_{ON} \uparrow$

- For Inductive loads t_r is high as compared to the resistive load becoz inductor limits the current rating and capacitor limits the voltage rating.

- Spread time → (t_s) It depends on the geometrical structure of device.

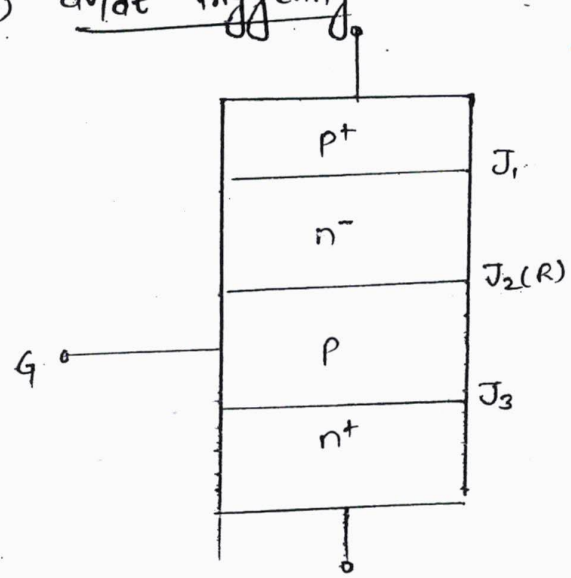
Turn ON time of SCR mainly depends on gate signal magnitude and load circuit parameters.

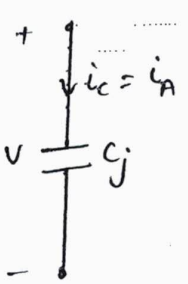
TURN ON METHODS →

1) Forward voltage triggering →

Not prefered

2) dv/dt triggering →



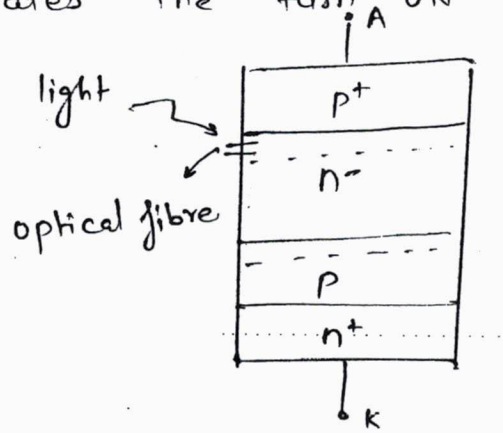


$$i_c = C_j \frac{dv}{dt}$$

- At high dv/dt the charging current increases if the ↑ in the charging current is more than the latching current then the SCR will turn ON.

③ light triggering →

When a light radiation in incident near the gate junction, the depletion layer absorb the light energy and produce more number of e^- and holes. This initiates the turn ON process.

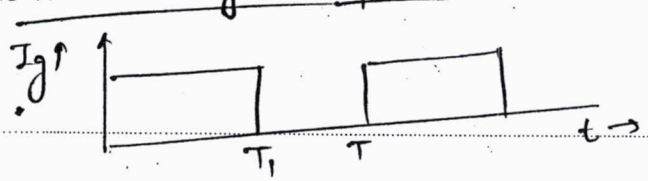


light triggering is more efficient and reliable to trigger multiple no. of SCR's simultaneously at a time.

Application → It is used in LASCR's for HVDC applications.

④ Gate triggering →

① Continous gate pulse →



- In this method we maintain the gate pulse width for a long duration of time until the SCR is required to remain in ON state.
- In this case power loss will increase.

$$\text{Power loss} = V_g I_g$$

$$V_g I_g \leq P_{gAV}$$

- P_{gAV} → It speficies the maximum limit for average gate power loss.